In the Claims

Please cancel claims 16-37 without prejudice.

Please add the following new claims:

--38. The apparatus of claim 1 wherein the VID-to-PID table is stored in a programmable register and the programmable register is loaded utilizing a DMA instruction.--

--39. The apparatus of claim 1 wherein the VID-to-PID table is stored in a programmable register and the programmable register loaded utilizing a direct write to the programmable register.--

--40. The apparatus of claim 9 wherein the translation logic comprises a translation vector.--

--41. The apparatus of claim 40 wherein the translation logic performs a logical operation utilizing the translation vector and a VID to generate a PID.--

--42. A processing apparatus comprising:

a plurality of processing elements (PEs) communicatively connected by a bus, each PE comprising a register storing a virtual identification number (VID) identifying the PE; and

a direct memory access (DMA) controller connected to the bus for accessing local data memory of the PEs, each data access at least partially identified by a VID;

wherein during a data access a PE responds to the data access if the VID stored in the register matches the VID of the data access.--

--43. The processing apparatus of claim 42 wherein each PE comprises a local memory interface unit (LMIU) which includes the register storing the VID.--

--44. The processing apparatus of claim 42 wherein the data access is a read access.--

--45. The processing apparatus of claim 42 wherein the data access is a write access.--

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